WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Wednesday, January 26, 2005

Hide?	Set Name	Query	Hit Count
	DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L27	l11 and l20	8
☐	L26	l9 and l20	2
☐	L25	l8 and l20	24
☐	L24	l4 and l20	2
☐	L23	l3 and l20	2
☐	L22	l1.ab. and L20	6
☐	L21	l1 and L20	44
☐	L20	l18 or L19	3454
☐	L19	340/635,636.1,636.19.ccls.	1282
☐	L18	713/300,322,340,600.ccls.	2183
☐	L17	((send$4 or output$4 or transfer$4 or transmit$4) near3 power near3 status) with parallel$	12
☐	L16	(receiv$4 near3 power near3 status) with serial$	3
☐	L15	L12.clm.	0
☐	L14	L12.ab.	1
☐	L13	L12 same parallel$4	1
☐	L12	L11 same clock$4	25
☐	L11	(power near2 status) same (buffer$4 or queu$4 or fifo)	157
☐	L10	L8 same (buffer$4 or queu$4 or fifo)	12
☐	L9	L8 same (buffer$4 or queu$4 or fifo)	12
☐	L8	L7 same (storage or memory)	156
☐	L7	L6 same control$4	580
☐	L6	(power adj status)	1066
☐	L5	l1 and L4	1
☐	L4	(deliver$4 or send$4 or transfer$4 or transmit$4 or output$4) near3 (power adj status) near3 signal$4	37
☐	L3	(send$4 or transfer$4 or transmit$4 or output$4) near3 (power adj status) near3 signal$4	36
☐	L2	L1 same (power near2 status)	8
☐	L1	(smart or intelligent) near2 battery	788

L9: Entry 1 of 12 File: USPT Oct 19, 2004

DOCUMENT-IDENTIFIER: US 6807188 B1
TITLE: Ranging arrangement and method for TDMA communications

Detailed Description Text (9):
Controller 205 includes central processor unit (CPU) 208 which may be a microprocessor, memory 209, user input/output (I/O) units 210, status register 211, assigned time slot register 212, start of down-stream frame register 213, ranging delay register 214, transmit burst control unit 215 and data first-in-first-out (FIFO) register 221. Units 206, 208 through 215 and 221 are interconnected via bus 207. A power ON status signal is supplied to one input of AND gate 216, while an initialized status signal is supplied to an inhibit input of AND gate 216, both from status register 211. Thus, And gate 216 yields a high state output when power ON is a high state and initialized is a low state. This high state output from AND gate 216 is supplied via OR gate 217 to enable ranging tone oscillator 220 to supply as an output the desired out-of-band ranging tone. In this manner the ranging state is effected. Again, in this example, the out-of-band ranging tone is generated at 466.56 MHz. This ranging tone is supplied to summer 222 and, thereafter, to PSPON 111 via E/O 204 and PSPON interface 202.

L9: Entry 5 of 12 File: USPT Mar 9, 1993

DOCUMENT-IDENTIFIER: US 5193176 A
TITLE: Computer work saving during power interruption

Detailed Description Text (15):
With respect to addressing the RAM 62 and the controller 66, the addresses occupy a window of 8 kilobytes and a lower range of megabyte of standard memory address space, as may be established with the aid of a buffer 132 and address jumpers 134. In the usual installation of the card 24 in a computer, such as the computer 20, the card would be addressed in auxiliary memory space. By way of example, the starting address for the card 24 would be the address CE000H. As noted above, the RAM 62 has sufficient storage space for storing a program for control of the power card 24, including the saving of data and restoration of the application program at the stage of operation which was present at the time of the power interruption. The preferred embodiment of the invention is advantageous in that no standard memory space is assumed by the program of the power card 24, and that only backup operating resources are used. This results in an independence of the backup operating system from the operating system of the host computer. By use of the bus 32, the power card 24 provides power status signals to the computer 20. The interface 62 and the buffer circuitry 130 can be employed with various computers and backup power circuits so that the invention is operative to support, for example, the use of a specific power circuit for different computer systems, simply by changing instructions stored in the RAM 62. The system can be arranged wherein the residual portion backup routine does not use operating system resources, only BIOS.

L9: Entry 6 of 12 File: USPT Mar 17, 1992

DOCUMENT-IDENTIFIER: US 5097249 A
TITLE: Power status detecting apparatus

Detailed Description Text (11):
FIG. 3 shows an example of a practical circuit arrangement of the power status detecting apparatus 11 shown in FIG. 1. The power status detecting apparatus 11 comprises a current detecting portion 20 which is connected to an analog-to-digital (A/D) converter 21. A micro-processor 22 is connected to the A/D converter 21 and is connected to a buffer memory 23 which stores an initial value of the power source currents which correspond to each of the equipments. A second buffer memory 24 which stores threshold current values corresponding to each of the equipments is also connected to the micro-processor 22 as also is a buffer memory 25 in which codes of various control signals of the respective equipments are stored as data bases. A fourth buffer memory 26 in which data corresponding to ports connected to the respective equipments are stored is also connected to micro-processor 22.

Detailed Description Text (18):
After the threshold values for identifying the power status of the respective equipments have been once determined as described above, the micro-processor 22 can easily identify the power status of the respective equipments on the basis of the outputs of the threshold buffer memory 24. In that case, in association with the buffer memory 26, the system control apparatus 12 can detect the relationship between the outlet 30 and the equipment which is connected thereto, if necessary.

Detailed Description Text (32):
Then, the processing of the micro-processor 22 proceeds to step 63, in which a threshold value which is used to identify the power status is computed on the basis of the previously-measured power source current value and is then stored in the buffer memory 24. The processing of the micro-processor 22 proceeds to the next decision step 64, in which it is determined whether or not the status of all of the ports have been determined. If the status of all ports have been determined as represented by a YES at step 64, then the processing of the micro-processor 22 ends. If on the other hand all ports have not yet been determined at step 64, then the processing of the micro-processor 22 proceeds to the next decision step 65. In step 65, it is determined whether or not the power status of all equipments have been checked. In other words, it is determined whether or not the power control signals have been generated for all equipments. If it is determined that all the equipments have not yet been checked as represented by a NO at step 65, then the processing of the micro-processor 22 returns to step 56. From step 56, the above-described operations are repeated. If it is determined that the checking of all the equipments has been finished as represented by a YES at step 65, then the processing of the micro-processor 22 ends.

L9: Entry 7 of 12 File: USPT May 10, 1988

DOCUMENT-IDENTIFIER: US 4744053 A
TITLE: ROM with mask programmable page configuration

Detailed Description Text (5):
Row decoder 12 receives its inputs directly from the output of an input buffer circuit, generally designated C. Column decoder 14 receives its inputs from page decoder 16 which, in turn, is connected to the output of a random access memory, generally designated D. RAM D is connected by means of parallel lines 18 to data transfer circuit B so as to receive the bits of the page address signal therefrom. It is also connected to the output of input buffer circuit C and to the output of a gate 20. Gate 20 receives, as one input, a command (write enable) signal (WE) from an input function decoder circuit, generally designated E. The output of the function generator E is also connected to decoder 16. The other input of gate 20 is the Chip Enable (CE) signal which is an input to input buffer circuit C, which is also connected to the power down circuitry 22 of conventional design. Gate 20 causes all of the storage devices in the non-selected pages of ROM A to be in the low power mode. Circuit 22 controls the power status of other circuits in the system.

L9: Entry 8 of 12 File: USPT Nov 7, 1978

DOCUMENT-IDENTIFIER: US 4124889 A
TITLE: Distributed input/output controller system

Detailed Description Text (332):
If the truth state of the signal on the Power status line S1 indicates that power had been applied to the device, the Acknowledge status line S2 is monitored (section 37) by the peripheral-unit controller for an Acknowledge signal in a logical zero state which indicates that the line printer is not processing a character previously transferred by the computer unit CU. If the Acknowledge line signal is in a logical one state, the peripheral-unit controller rechecks power and again monitors the Acknowledge line. This iterative process is repeated until the signal on the Acknowledge line S2 becomes a logical zero, indicating that the line printer has completed processing the previously transferred data character and is now ready for a subsequent transfer. When the signal on the Acknowledge line S2 becomes a logical zero, the peripheral-unit controller generates a data-service interrupt signal (section 38) that is transferred to the multiplexer MUX over the input/output bus IOB. When top priority is attained, the interrupt signal is vectored to programmed, preselected memory cells in the main memory unit MMU of the computer unit CU. The central processor unit CPU then executes an automatic output instruction and places data on the data bus DB and the decrements the transfer count and the memory buffer address in the assigned locations of the main memory unit MMU (section 39).

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L16: Entry 1 of 3 File: USPT Nov 7, 1995

DOCUMENT-IDENTIFIER: US 5465011 A
TITLE: Uninterruptible power supply with improved output regulation

Abstract Text (1):
A microprocessor based uninterruptible power supply generates an AC electrical output power from an AC input source when the AC input source is within settable voltage limits and from an auxiliary source of DC power when the AC input source is outside said the voltage limits. The microprocessor provides monitoring of the AC input voltage to determine its amplitude and frequency, and uses this information to set the magnitude and frequency of the AC output voltage and to select the source of the AC output power. A power factor improvement circuit boosts the selected source to a high DC voltage which is inverted by a chopper circuit to produce a high frequency AC voltage is rectified and sent to a PWM inverter to produce the AC output power. An average current feedback loop provides the output voltage regulation and utilizes current limiting to provide output current limiting for protection against short circuits and overloads. A voltage phase relationship is maintained between the AC input power and AC output power to eliminate voltage and current transients at transfer times between the AC and DC input sources. A serial data communications port sends data sent over a network that includes signals indicative of the status of the uninterruptible power supply and receives data from the network for controlling operation of the uninterruptible power supply.

CLAIMS:

19. The method of claim 17 further including exchanging data over a serial data communications network wherein said data sent over said network includes signals indicative of the status of said uninterruptible power supply and said data received over said network includes signals for controlling operation of said uninterruptible power supply.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L22: Entry 3 of 6 File: USPT May 22, 2001

DOCUMENT-IDENTIFIER: US 6236326 B1
TITLE: Method and apparatus for intelligently signaling a battery charge condition in a wireless telephone

Abstract Text (1):
An apparatus and method for intelligent low battery response by a wireless telephone is provided. When the wireless telephone's rechargeable battery nears depletion of energy, and a call is in progress, the party conversing with the wireless telephone user is provided with a voice notification that termination of the call due to battery depletion is imminent. When the wireless telephone's rechargeable battery pack nears depletion of energy and a call is not in progress, the wireless telephone automatically initiates call forwarding with the wireless telephone network such that calls directed to the subscriber's wireless telephone number while the battery is depleted are redirected to a different telephone number. After replacing or recharging a depleted battery pack, and repowering on the wireless telephone, call forwarding is automatically deactivated such that the subscriber can resume receiving calls at the wireless telephone number.

Current US Original Classification (1):
340/636.1

Current US Cross Reference Classification (3):
340/635

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L2: Entry 1 of 8 File: USPT Jan 21, 2003

DOCUMENT-IDENTIFIER: US 6509717 B2
TITLE: Smart battery, secondary smart battery connection apparatus of portable computer system, AC adapter implementing same, and connection method thereof

CLAIMS:

28. In a smart battery including a rechargeable electrical power source and internal circuitry for the communication of control and status data of the rechargeable electrical power source and having a first connector provided on an exterior of said smart battery for enabling said smart battery to be connected to other devices for supplying and/or receiving electrical power thereto and/or therefrom and for enabling communication of status and control data therewith, the smart battery comprising: a second connector provided on the exterior of said smart battery, for connecting with the first connector of the second smart battery, said second connector of said smart battery routing electrical power and status and control data signals between said first connector of said smart battery and said first connector of said second smart battery when said second smart battery is connected to the second connector of said smart battery.

29. The smart battery according to claim 28, further comprising: a switching circuit within said smart battery operable to selectively route to/from said first connector of said smart battery electrical power and status and control signaled from/to said smart battery and power and status and control signals from/to a second smart battery connected to said second connector of said smart battery.

Previous Doc Next Doc Go to Doc#

L2: Entry 2 of 8 File: USPT Jan 21, 2003

DOCUMENT-IDENTIFIER: US 6509657 B1
TITLE: Battery backup unit system and interface

Detailed Description Text (21):
FIG. 6 is flow diagram of a method 120 of communicating power-related information to the motherboard 20. The battery backup unit 14 can be configured to detect various changes in the status of the power supply unit 12, the battery pack 16, and/or the battery backup unit 14 itself (122). Such changes can include, for example, the insertion or removal of the battery pack 16 or battery 26, overheating of the battery 26, or an indication that there has been a loss of AC power. When such a change is detected, the microcontroller 22 can be configured to update any information stored in the EEPROM 40 (or smart battery, if one is used) related to that change (124) and/or assert an interrupt on the motherboard 20 (126). Then, the battery backup unit 14 supplies status information to the motherboard 20 if and when requested by the motherboard 20 (128, 130).

L2: Entry 4 of 8 File: USPT Apr 24, 2001

DOCUMENT-IDENTIFIER: US 6222347 B1
** See image for Certificate of Correction **
TITLE: System for charging portable computer's battery using both the dynamically determined power available based on power consumed by sub-system devices and power limits from the battery

Detailed Description Text (10):
In one implementation, the battery 104 is a "smart battery" that is able to monitor its own condition. More particularly, the battery 104 includes a battery monitor 112 that monitors the condition of the battery 104 and supplies digital signals to other components of the computer system that are interested in monitoring the conditions of the battery 104. In the embodiment illustrated in FIG. 1, the battery monitor 112 forwards a charge request and status information to the power management microprocessor 106 . The charge request, for example, includes a maximum charge current and a maximum charge voltage that the battery 104 desires to receive for the purpose of charging the battery 104. Typically, these maximum values are associated with the chemical composition of the battery 104 and thus can vary from battery to battery. The status information, for example, includes battery voltage, battery temperature, and capacity (e.g., percentage charged or discharged). In any event, the power management microprocessor 106 receives the charge request and the status information from the battery monitor 112, and then processes the information to determine a suitable charge current (I_CHRG) and a charge voltage (V_CHRG).

L2: Entry 5 of 8 File: USPT Feb 15, 2000

DOCUMENT-IDENTIFIER: US 6025698 A
TITLE: Smart battery charging system, charging method therefor and power supply system for portable computer using the same

Brief Summary Text (24):
A power supply system for a notebook computer, according to a fifth aspect of the present invention, includs a smart battery that has a positive port (+), a resistance sensing port T, a SM bus data port D, a SM bus clock port C and a negative port (-), and outputs various data, such as over charged alarm, charge terminated alarm, over temperature alarm, fully charged alarm and fully discharged alarm through SM bus data port T and SM bus clock port C. The notebook computer charges the smart battery when an external power source is connected thereinto, and utilizes the charging power of the smart battery as an operational power when no external power source is connected thereinto. A power input means is connected to the external power source and a positive port of the smart battery, for outputting external power or smart battery power selectively based on the connection status of the external power source and outputting the external power as a first power voltage. A power on-off signal input means through which a user turns on and off the notebook computer. A SMPS for outputting a second power voltage for operating the notebook computer based on the operational power obtained from the power input means when the notebook computer is turned on, and outputting a first level of power good signal when power is on and a second level of power good signal when power is off. A constant voltage regulating means generates a third power, based on the second power voltage when the power good signal is the first level, and based on the first power voltage when the power good signal is the second level. A battery charging means, utilizes the first power voltage as an operational power and includes a charging power output port connected to the positive port of the smart battery, for varying voltage level and current level of the charging power, ouputted through the charging power output port, according to data inputted through an SM bus. A keyboard controller, utilizes the third power voltage as an operational power and connects to the battery caring means and the smart battery through the SM bus, for controlling the smart battery charging means by identifying the type of smart battery based on battery identifying signals obtained from a charge signal generating means.

Brief Summary Text (28):
Moreover, the power supply system, in accordance with the present invention, sets the charging power for the smart battery appropriately according, to the on-off status of the notebook computer, and outputs a save-to-disk signal STD based on the charge amount of the smart battery and the connection status of the external power, thus enhancing the security in operations of the notebook computer.

Detailed Description Text (69):
FIG. 10 shows a bit configuration of the battery flag register of 8-bit data. Bit 0 and 1 of the battery flag register express the charge status of the smart battery 70, where the bit value "00" represents a battery normal status that the charge amount of the smart battery 70 is about 11 to 100%, the bit value "01" means a battery exhausted status that the charged amount is about 6 to 10%, and the bit value "10" denotes a battery dried-up status that the charge amount is less than or equal to 5%. Bit 2 expresses the charge status of the smart battery 70, where the

bit value "1"represents that the smart battery 70 is not fully charged and the bit value "0" means that the smart battery 70 is fully charged. Bit 3 expresses the present operational status of the smart battery 70, where the bit value "1"represents a suspend mode and "0" means a normal mode. Bit 4 is not used. Bit 5 expresses the present charge status of the smart battery 70, where the bit value "1" represents that the charging is terminated and "0" denotes that the charging is in progress. Bit 6 expresses the types of smart batteries connected to the notebook computer, where the bit value "1"represents Li-ion smart battery and "0" means Ni-MH smart battery. Bit 7 expresses the present external power status, the bit value "1"represents that AC power is inputted from the power input port 121 of FIG. 8 and "0" means that AC power is not inputted.

Detailed Description Text (70):
Meanwhile, in the memory provided in the keyboard controller 80, various status data and control data, such as LiIon.sub.-- Volt, that is, voltage regulating data of charging power V.sub.CH applied from the smart battery charger 60 to the smart battery 70, and APM.sub.-- RSOC.sub.-- STATUS for advanced power management of Windows 95. In fact, the LiIon.sub.-- Volt corresponds to the data value for setting the charging voltage, supplied from the smart battery charger 60 to the smart battery 70, that is, the data value applied to the digital-to-analog converter 50, however, hereinafter, the value of LiIon.sub.-- Volt will be defined as the charging voltage value supplied to the smart battery 70 so as to explain in brief.

Detailed Description Text (96):
Meanwhile, at steps 75 and 82, if AC power is not inputted, that is, if a user turns on the power switch when an external power source is not connected, the keyboard controller 80 executes various data process for secure operations of notebook computer based on power status of the smart battery 70.

Detailed Description Text (98):
Here, when an external power source is not connected to the notebook computer, as described in FIG. 8, the smart battery charger 60 is set to a non-operational status according as the first power voltage V1 is not outputted from the power input part 120. Nevertheless, the reason the keyboard controller 80 controls the smart battery charger 60 to set the charging voltage to a predetermined value, that is, a reference value, is to provide against a case that the system returns to the step 140 due to an error of the system when an external power is inputted, or a case that the external power is inputted in a sudden when the user uses the notebook computer. That is, at steps 140 to 147, the system can provide for an abnormal operation by resetting the smart battery charger 60 to supply the minimum charging power to the smart battery 70 according to the charge status and the type of the smart battery 70.

Detailed Description Text (103):
Moreover, the power supply system, in accordance with the present invention, sets the charging power for the smart battery appropriately according to the on-off status of the notebook computer, and outputs a save-to-disk signal STD based on the charge amount of the smart battery and the connection status of the external power, thus enhancing the security in operations of the notebook computer.

CLAIMS:

8. A power including a smart battery that has a positive port (+), a resistance sensing port T, a System Management SM bus data port D, a System Management SM bus clock port C and a negative port (-), and outputs various data, such as over charged alarm, charge terminated alarm, over temperature alarm, fully charged alarm and fully discharged alarm through SM bus data port T and SM bus clock port C, the notebook computer charges the smart battery in case that an external power source is connected thereinto, and utilizes the charging power of the smart battery as an

L2: Entry 6 of 8 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 5998972 A
TITLE: Method and apparatus for rapidly charging a battery of a portable computing device

Detailed Description Text (8):
In one implementation, the battery 104 is a "smart battery" that is able to monitor its own condition. More particularly, the battery 104 includes a battery monitor 112 that monitors the condition of the battery 104 and supplies digital signals to other components of the computer system that are interested in monitoring the conditions of the battery 104. In the embodiment illustrated in FIG. 1, the battery monitor 112 forwards a charge request and status information to the power management microprocessor 106. The charge request, for example, includes a maximum charge current and a maximum charge voltage that the battery 104 desires to receive for the purpose of charging the battery 104. Typically, these maximum values are associated with the chemical composition of the battery 104 and thus can vary from battery to battery. The status information, for example, includes battery voltage, battery temperature, and capacity (e.g., percentage charged or discharged). In any event, the power management microprocessor 106 receives the charge request and the status information from the battery monitor 112, and then processes the information to determine a suitable charge current (I.sub.-- CHRG) and a charge voltage (V.sub.-- CHRG).

L2: Entry 7 of 8 File: USPT May 19, 1998

DOCUMENT-IDENTIFIER: US 5754868 A
TITLE: Electronic apparatus having conventional and battery power sources, and having a battery discharge mode wherein a first portion of the apparatus is powered by the conventional power source and a second portion of the apparatus is powered by the battery

Detailed Description Text (12):
The extended I/O controller 26 is a peripheral LSI by which a pointing device 32, an RTC (Real Time Clock)/CMOS 33, an EEPROM (Electrically Erasable PROM) 34, and a power controller 35 communicate with the extended I/O bus 14. The pointing device 32 is a coordinate input means, such as a mouse or a joy stick. The CMOS 33 is a memory device where data for the system configuration are temporarily stored. In this embodiment, the CMOS 33 and the RTC are packaged in the same chip. The EEPROM 34 is a nonvolatile memory device in which are stored data required for maintaining the secrecy of information for the system 10, such as a password. The power controller 35 monitors the terminal voltage of the battery 3 (the remaining capacity of the battery 3 if it is an intelligent battery) or a matrix entered through a keyboard 36 and controls the supply of power to the system 10. More specifically, the power controller 35 outputs a control signal that is employed to turn on or off the switches SW1, SW2, SW-A, and SW-B, which are located on the power lines that extend from the AC power source 2 and the battery pack 3 to the system 10 (see FIG. 2). The power controller 35 then starts or terminates the discharge of the battery 3, or, upon the request of a user, performs the full discharge of the battery 3 (this process will be described later). In addition, the power controller 35 permits an LED status indicator 37 to display the current power supply status of the system 10 (e.g., in the suspended status, in the charged status, or in a low-battery status).

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L17: Entry 2 of 12 File: USPT May 26, 1998

DOCUMENT-IDENTIFIER: US 5758171 A
TITLE: Apparatus and method for reading back socket power status information

CLAIMS:

1. A computer system for controlling and monitoring power and temperature status and rapidly responding to indicated abnormalities in power or temperature of at least one externally removable card, comprising:

a power control circuit, coupled to the at least one externally removable card, for providing at least one voltage supply to the at least one externally removable card and for monitoring at least one condition of the power control circuit; and

an interface circuit, coupled to the at least one externally removable card by a set of parallel data and control lines, a host processor by a system data and control bus, and the power control circuit by a system management bus, for transmitting and receiving data and control signals to and from the at least one externally removable card and the host processor, and for receiving, from the power control circuit, status data indicating the at least one condition of the power control circuit and transmitting, in response to received status data, a signal to the power control circuit for controlling the at least one voltage supply to the at least one externally removable card, each of which transmitting and receiving is performed by the respectively coupling bus or lines.

Previous Doc Next Doc Go to Doc#